Part – B

1. Explain the formation of depletion layer in PN junction

Electrons and holes diffuse into regions with lower concentrations of electrons and holes, much as ink diffuses into water until it is uniformly distributed. By definition, N-type semiconductor has an excess of free electrons compared to the P-type region, and P-type has an excess of holes compared to the N-type region. Therefore when N-doped and P-doped pieces of semiconductor are placed together to form a junction, electrons migrate into the P-side and holes migrate into the N-side. Departure of an electron from the N-side to the P-side leaves a positive donor ion behind on the N-side, and likewise the hole leaves a negative acceptor ion on the P-side.

![Diagram of PN junction with depletion regions](image)

The diffused electrons come into contact with holes on the P-side and are eliminated by recombination. Likewise for the diffused holes on the N-side. The net result is the diffused electrons and holes are gone, leaving behind the charged ions adjacent to the interface in a region with no mobile carriers (called the depletion region). The uncompensated ions are positive on the N side and negative on the P.
side. This creates an electric field that provides a force opposing the continued exchange of charge carriers. When the electric field is sufficient to arrest further transfer of holes and electrons, the depletion region has reached its equilibrium dimensions. Integrating the electric field across the depletion region determines what is called the built-in voltage (also called the junction voltage or barrier voltage or contact potential.

2. **Discuss the behavior of PN junction when it is**

   (I) **Forward Biased**

   (II) **Reverse Biased**

**Forward Bias:**

In forward bias, the p-type is connected with the positive terminal and the n-type is connected with the negative terminal. With a battery connected this way, the holes in the P-type region and the electrons in the N-type region are pushed toward the junction. This reduces the width of the depletion zone.

The positive potential applied to the P-type material repels the holes, while the negative potential applied to the N-type material repels the electrons. As electrons and holes are pushed toward the
junction, the distance between them decreases. This lowers the barrier in potential. With increasing forward-bias voltage, the depletion zone eventually becomes thin enough that the zone's electric field cannot counteract charge carrier motion across the p–n junction, as a consequence reducing electrical resistance. The electrons that cross the p–n junction into the P-type material (or holes that cross into the N-type material) will diffuse in the near-neutral region. Therefore, the amount of minority diffusion in the near-neutral zones determines the amount of current that may flow through the diode.

**Reverse Bias:**

Connecting the *P-type* region to the *negative* terminal of the battery and the *N-type* region to the *positive* terminal corresponds to reverse bias. If a diode is reverse-biased, the voltage at the cathode is comparatively higher than the anode. Therefore, no current will flow until the diode breaks down. The connections are illustrated in the diagram to the right.

Because the p-type material is now connected to the negative terminal of the power supply, the 'holes' in the P-type material are pulled away from the junction, causing the width of the depletion zone
to increase. Likewise, because the N-type region is connected to the positive terminal, the electrons will also be pulled away from the junction. Therefore, the depletion region widens, and does so increasingly with increasing reverse-bias voltage. This increases the voltage barrier causing a high resistance to the flow of charge carriers, thus allowing minimal electric current to cross the p–n junction. The increase in resistance of the p–n junction results in the junction behaving as an insulator.

3. Draw the VI Characteristics of PN junction diode and Explain

The operation of diodes (as with other semiconductor devices) is often described by a special graph called a "characteristic curve". These graphs show the relationship between the currents and voltages associated with the different terminals of the device.

The axes of the graph show both positive and negative values and so intersect at the centre. The intersection has a value of zero for both current (the Y axis) and voltage (the X axis). The axes +I and +V (top right) show the current rising steeply after an initial zero current
area. This is the forward conduction of the diode when the anode is positive and cathode negative. Initially no current flows until the applied voltage is at about the forward junction potential, after which current rises steeply showing that the forward resistance (I/V) of the diode is very low; a small increase in voltage giving a large increase in current.

The -V and -I axes show the reverse biased condition (bottom left). Here we see that although the voltage increases hardly any current flows. This small current is called the leakage current of the diode and is typically only a few micro-amps with germanium diodes and even less in silicon. If a high enough reverse voltage is applied however there is a point (called the reverse breakdown voltage) where the insulation of the depletion layer breaks down and a very high current suddenly flows. In most diodes this breakdown is permanent and a diode subjected to this high reverse voltage will be destroyed.

4. Draw the circuit diagram of half wave rectifier? Explain its working?
What the frequency of ripple in its output?

Circuit Diagram:

**Working:**

The half wave rectifier will allow only the positive half cycles and omit the negative half cycles.
Positive Half Cycle:
- In the positive half cycles when the input AC power is given to the primary winding of the step down transformer, we will get the decreased voltage at the secondary winding which is given to the diode.
- The diode will allow current flowing in clock wise direction from anode to cathode in the forward bias (diode conduction will take place in forward bias) which will generate only the positive half cycle of the AC.
- The diode will eliminate the variations in the supply and give the pulsating DC voltage to the load resistance $R_L$. We can get the pulsating DC at the Load resistance.

Negative Half Cycle:
- In the negative half cycle the current will flow in the anti-clockwise direction and the diode will go in to the reverse bias. In the reverse bias the diode will not conduct so, no current in flown from anode to cathode, and we cannot get any power at the load resistance.
- Only small amount of reverse current is flown from the diode but this current is almost negligible. And voltage across the load resistance is also zero.
Ripple factor:

It is defined as the amount of AC content in the output DC. It nothing but amount of AC noise in the output DC. Less the ripple factor, performance of the rectifier is more. The ripple factor of half wave rectifier is about 1.21 (full wave rectifier has about 0.48). It can be calculated as follows:

The effective value of the load current \( I \) is given as sum of the rms values of harmonic currents \( I_1, I_2, I_3, I_4 \) and DC current \( I_{dc} \).

\[
I^2 = I_{dc}^2 + I_1^2 + I_2^2 + I_4^2 = I_{dc}^2 + I_{ac}^2
\]

Ripple factor, is given as

\[
\gamma = \frac{I_{ac}}{I_{dc}} = \frac{(I^2 - I_{dc}^2)}{I_{dc}} = \left\{ \left( \frac{I_{rms}}{I_{dc}} \right)^2 - 1 \right\} = Kf^2 - 1
\]

Where \( Kf \) is the form factor of the input voltage.

Form factor is given as \( Kf = \frac{I_{rms}}{I_{avg}} = \frac{(I_{max}/2)}{(I_{max}/\pi)} = \pi/2 = 1.57 \)

So, ripple factor, \( \gamma = (1.57^2 - 1) = 1.21 \)

Half wave rectifier is mainly used in the low power circuits.

It has very low performance compared with the other rectifiers.

5. Derive the relation between alpha and beta

Relation between alpha and Beta is derived from the common Emitter and Common Base configuration
By combining the expressions for both Alpha, $\alpha$ and Beta

$$\text{Alpha, } (\alpha) = \frac{I_C}{I_E} \quad \text{and} \quad \text{Beta, } (\beta) = \frac{I_C}{I_B}$$

$$\therefore I_C = \alpha \cdot I_E = \beta \cdot I_B$$

as: $$\alpha = \frac{\beta}{\beta + 1} \quad \beta = \frac{\alpha}{1 - \alpha}$$

$$I_E = I_C + I_B$$

Where: “$I_c$” is the current flowing into the collector terminal, “$I_b$” is the current flowing into the base terminal and “$I_e$” is the current flowing out of the emitter terminal.

This type of bipolar transistor configuration has a greater input impedance, current and power gain than that of the common base configuration but its voltage gain is much lower. The common emitter configuration is an inverting amplifier circuit. This means that the resulting output signal is $180^\circ$ “out-of-phase” with the input voltage signal.
6. Discuss the DC load line analysis of a bipolar transistor

Load line is used in graphical analysis of usually drawn on a graph of the current vs the voltage in the nonlinear device, called the device's characteristic curve. A load line, usually a straight line, represents the response of the linear part of the circuit, connected to the nonlinear device in question. The operating point(s) of the circuit are the points where the characteristic curve and the load line intersect; at these points the current and voltage parameters of both parts of the circuit match.

The characteristic curve (*curved line*), representing current \( I \) is an exponential curve. The load line (*diagonal line*) represents the relationship between current and voltage due to Kirchhoff's voltage law applied to the resistor and voltage source, is

In a BJT circuit, the BJT has a different current-voltage \((I_C-V_{CE})\) characteristic depending on the base current. Placing a series of these curves on the graph shows how the base current will affect the operating point of the circuit.

\[
\text{When: } (V_{CE} = 0) \quad I_C = \frac{V_{CC} - 0}{R_L}, \quad I_C = \frac{V_{CC}}{R_L}
\]

\[
\text{When: } (I_C = 0) \quad 0 = \frac{V_{CC} - V_{CE}}{R_L}, \quad V_{CC} = V_{CE}
\]
7. Explain the concept of Voltage divider bias method

Voltage Divider Transistor Biasing

The common emitter transistor is biased with the two resistors $R_{B1}$ and $R_{B2}$ connected to the transistor's base terminal across the supply.

This voltage divider configuration is the most widely used transistor biasing method, as the emitter diode of the transistor is
forward biased by the voltage dropped across resistor $R_{B2}$. Also, voltage divider network biasing makes the transistor circuit independent of changes in beta as the voltages at the transistors base, emitter, and collector are dependent on external circuit values.

To calculate the voltage developed across resistor $R_{B2}$ and therefore the voltage applied to the base terminal uses the voltage divider formula for resistors in series. The current flowing through resistor $R_{B2}$ is generally set at 10 times the value of the required base current $I_B$ so that it has no effect on the voltage divider current or changes in Beta.

The goal of Transistor Biasing is to establish a known Q-point in order for the transistor to work efficiently and produce an undistorted output signal. Correct biasing of the transistor also establishes its initial AC operating region with practical biasing circuits using either a two or four-resistor bias network.

In bipolar transistor circuits, the Q-point is represented by $(V_{CE}, I_C)$ for the NPN transistors or $(V_{EC}, I_C)$ for PNP transistors. The stability of the base bias network and therefore the Q-point is generally assessed by considering the collector current as a function of both Beta ($\beta$) and temperature.

8. Explain the working principle of a transistor as an amplifier

Common Emitter Amplifier Circuit

Transistor Amplifiers operates using AC signal inputs which alternate between a positive value and a negative value so some way of “presetting” the amplifier circuit to operate between these two
maximum or peak values is required. This is achieved using a process known as Biasing. Biasing is very important in amplifier design as it establishes the correct operating point of the transistor amplifier ready to receive signals, thereby reducing any distortion to the output signal.

The aim of any small signal amplifier is to amplify all of the input signal with the minimum amount of distortion possible to the output signal, in other words, the output signal must be an exact reproduction of the input signal but only bigger (amplified).

To obtain low distortion when used as an amplifier the operating quiescent point needs to be correctly selected. This is in fact the DC operating point of the amplifier and its position may be established at any point along the load line by a suitable biasing arrangement. The best possible position for this Q-point is as close to the center position of the load line as reasonably possible, thereby producing a Class A type amplifier operation, ie.

\[ V_{ce} = \frac{1}{2} V_{cc} \]

Consider the Common Emitter Amplifier circuit shown below.

The Common Emitter Amplifier Circuit
The single stage common emitter amplifier circuit shown above uses what is commonly called “Voltage Divider Biasing”. This type of biasing arrangement uses two resistors as a potential divider network across the supply with their center point supplying the required Base bias voltage to the transistor. Voltage divider biasing is commonly used in the design of bipolar transistor amplifier circuits.

This method of biasing the transistor greatly reduces the effects of varying Beta, (\( \beta \)) by holding the Base bias at a constant steady voltage level allowing for best stability. The quiescent Base voltage (\( V_b \)) is determined by the potential divider network formed by the two resistors, R1, R2 and the power supply voltage \( V_{cc} \) as shown with the current flowing through both resistors.

Then the total resistance \( R_T \) will be equal to \( R_1 + R_2 \) giving the current as \( i = \frac{V_{cc}}{R_T} \). The voltage level generated at the junction of resistors R1 and R2 holds the Base voltage (\( V_b \)) constant at a value below the supply voltage.

Then the potential divider network used in the common emitter amplifier circuit divides the input signal in proportion to the resistance. This bias reference voltage can be easily calculated using the simple voltage divider formula below:
\[ V_B = \frac{V_{CC} \cdot R_2}{R_1 + R_2} \]

The supply voltage (Vcc) determines the maximum Collector current, \( I_c \) when the transistor is switched fully “ON” (saturation), \( V_{ce} = 0 \). The Base current \( I_B \) for the transistor is found from the Collector current, \( I_c \) and the DC current gain Beta, \( \beta \) of the transistor.

\[ \beta = \frac{\Delta I_C}{\Delta I_B} \]

9. Illustrate Class A Amplifier in detail

Class A, “the best class” of amplifier due mainly to their low signal distortion levels and are probably the best sounding of all the amplifier classes. The class A amplifier has the highest linearity over the other amplifier classes and as such operates in the linear portion of the characteristics curve.

Class A amplifiers use the same single transistor (Bipolar, FET, IGBT, etc) connected in a common emitter configuration for both halves of the waveform with the transistor always having current flowing through it, even if it has no base signal.

To achieve high linearity and gain, the output stage of a class A amplifier is biased “ON” (conducting) all the time. Then for an amplifier to be classified as “Class A” the zero signal idle current in the output stage must be equal to or greater than the maximum load
current (usually a loudspeaker) required to produce the largest output signal.

As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform. Then the class A amplifier is equivalent to a current source.

Since a class A amplifier operates in the linear region, the transistors base (or gate) DC biasing voltage should by chosen properly to ensure correct operation and low distortion. However, as the output device is “ON” at all times, it is constantly carrying current, which represents a continuous loss of power in the amplifier.

**Efficiency Calculation:**

Thus power input to the transistor, $P_{tr} = $ Power drawn from collector supply, $P_{in\,(dc)} = V_{CC}I_{CQ}$ and overall efficiency becomes equal to collector efficiency and $\eta = P_{out\,(ac)}/ V_{CC}\times I_{CQ}$

Under condition of development of maximum ac power, voltage swings from $V_{ce\,max}$ to zero and collector current from $I_{c\,max}$ to zero. So

$$V_{rms} = 1/\sqrt{2} \{ [V_{ce\,max} - V_{ce\,min}]/2 \}$$

$$= V_{ce\,max}/2\sqrt{2} = 2V_{CC}/2\sqrt{2} = V_{CC}/\sqrt{2}$$ And
\[ I_{\text{rms}} = \frac{1}{\sqrt{2}} \left\{ I_{c_{\text{max}}} - I_{c_{\text{min}}} \right\}/2 \]
\[ = I_{c_{\text{max}}/2\sqrt{2}} = 2I_{\text{CQ}}/2\sqrt{2} = I_{\text{CQ}}/\sqrt{2} \]

AC power developed across the load,
\[ P_{\text{out (ac)}} = V_{\text{rms}} I_{\text{rms}} = (V_{\text{CC}} I_{\text{CQ}})/2 \]

Collector efficiency = \( P_{\text{out (ac)}}/ (V_{\text{CC}} I_{\text{CQ}})/2 \div V_{\text{CC}} I_{\text{CQ}} \) = 0.5 or 50%.

Thus for a transformer-coupled class A power amplifier the maximum theoretical efficiency is 50%. In practice, the efficiency of such an amplifier is somewhat less than 50%. It is about 30%.

The efficiency of a transformer-coupled class A power amplifier can be given as
\[ \text{Efficiency} = 50 \times \{ [V_{\text{ce_{max}}} - V_{\text{ce_{min}}}] / [V_{\text{ce_{max}}} + V_{\text{ce_{min}}}] \} \% \]

The larger the value of \( V_{\text{ce_{max}}} \) and smaller the value of \( V_{\text{ce_{min}}} \) the closer the efficiency approaches the theoretical limit of 50%. Well-designed circuits can approach the limit of 50%.

10. List the properties of negative feedback.

<table>
<thead>
<tr>
<th>Stabilization of voltage gain</th>
<th>Decreasing output impedance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increasing input impedance</td>
<td>Decreasing distortion</td>
</tr>
<tr>
<td>Increasing bandwidth</td>
<td></td>
</tr>
</tbody>
</table>
The stabilization of the voltage gain of an amplifier against changes in the components (e.g., with temperature, frequency etc.,)

The input impedance is $\frac{v_{in}}{i_{in}}$ which without negative feedback is $Z_{in0}$.

But with feedback, the current is reduced to

$$i_{in} = \frac{v}{Z_{ino}} = \frac{v_{in} - Bv_{out}}{Z_{ino}}$$

The input voltage $v_{in}$ must be held constant while we see how $v_{out}$ varies with $i_{out}$. The easiest way to do this is with the partial derivative

$$Z_{out} = \frac{\partial v_{out}}{\partial i_{out}} = \frac{Z_{out}}{1 + \Delta_{0}B}$$

This decreases the impedance by a factor of 10 to 100 in transistor circuits and to practically zero in op-amps.

Discriminate against sources of noise or distortion within an amplifier. Considering a two-stage amplifier (after Simpson) with sources of distortion $v_{d1}$ and $v_{d2}$ inside the feedback loop.

Amplifier gain will generally decrease at higher frequencies, but the contribution of negative feedback in stabilizing voltage gain and making it nearly independent of the open-loop gain is a major contribution to extending the useful frequency range of amplifiers.

The input impedance is $\frac{v_{in}}{i_{in}}$ which without negative feedback is $Z_{in0}$.

But with feedback, the current is reduced to

$$i_{in} = \frac{v_{in}}{Z_{ino}} = \frac{v_{in} - Bv_{out}}{Z_{ino}}$$
11. With neat circuit diagram explain Hartley Oscillator

Hartley Oscillator Tank Circuit

In the **Hartley Oscillator** the tuned LC circuit is connected between the collector and the base of a transistor amplifier. As far as the oscillatory voltage is concerned, the emitter is connected to a tapping point on the tuned circuit coil.

The feedback part of the tuned LC tank circuit is taken from the centre tap of the inductor coil or even two separate coils in series which are in parallel with a variable capacitor, C as shown.

The Hartley circuit is often referred to as a split-inductance oscillator because coil L is centre-tapped. In effect, inductance L acts like two separate coils in very close proximity with the current flowing through coil section XY induces a signal into coil section YZ below.
When the circuit is oscillating, the voltage at point X (collector), relative to point Y (emitter), is $180^\circ$ out-of-phase with the voltage at point Z (base) relative to point Y. At the frequency of oscillation, the impedance of the Collector load is resistive and an increase in Base voltage causes a decrease in the Collector voltage. Then there is a $180^\circ$ phase change in the voltage between the Base and Collector and this along with the original $180^\circ$ phase shift in the feedback loop provides the correct phase relationship of positive feedback for oscillations to be maintained.

The amount of feedback depends upon the position of the “tapping point” of the inductor. If this is moved nearer to the collector the amount of feedback is increased, but the output taken between the Collector and earth is reduced and vice versa. Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitors act as DC-blocking capacitors.

The frequency of oscillation of the Hartley Oscillator being given as.

$$f = \frac{1}{2\pi \sqrt{L_T C}}$$

where: $L_T = L_1 + L_2 + 2M$

$L_T$ is the total cumulatively coupled inductance, mutual inductance $M$.

The frequency of oscillations can be adjusted by varying the “tuning” capacitor.
12. Distinguish between Bipolar and Unipolar Transistor

<table>
<thead>
<tr>
<th></th>
<th>JFET</th>
<th>BJT</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).</td>
<td>Bipolar device (current condition, by both types of carriers, i.e., majority and minority-electrons and holes)</td>
</tr>
<tr>
<td>2</td>
<td>The operation depends on the control of a junction depletion width under reverse bias.</td>
<td>The operation depends on the injection of minority carriers across a forward biased junction.</td>
</tr>
<tr>
<td>3</td>
<td>Voltage driven device. The current through the two terminals is controlled by a voltage at the third terminal (gate).</td>
<td>Current driven device. The current through the two terminals is controlled by a current at the third terminal (base).</td>
</tr>
<tr>
<td>4</td>
<td>Low noise level.</td>
<td>High noise level.</td>
</tr>
<tr>
<td>5</td>
<td>High input impedance (due to reverse bias).</td>
<td>Low input impedance (due to forward bias).</td>
</tr>
<tr>
<td>6</td>
<td>Gain is characterised by transconductance.</td>
<td>Gain is characterised by voltage gain.</td>
</tr>
<tr>
<td>7</td>
<td>Better thermal stability.</td>
<td>Less thermal stability.</td>
</tr>
</tbody>
</table>

13. Explain how SCR works as a switch
In this mode of operation, the anode is given a positive potential while the cathode is given a negative voltage, keeping the gate at zero potential i.e. disconnected. In this case junction J1 and J3 are forward biased while J2 is reversed biased due to which only a small leakage current exists from the anode to the cathode until the applied voltage reaches its break over value, at which J2 undergoes avalanche breakdown and at this break over voltage it starts conducting, but below break over voltage it offers very high resistance to the current and is said to be in the off state.

SCR can be brought from blocking mode to conduction mode in two ways: either by increasing the voltage across anode to cathode beyond break over voltage or by applying of positive pulse at gate. Once it starts conducting, no more gate voltage is required to maintain it in the on state. There is one way to turn it off. Reduce the current through it below a minimum value called the holding current.

SCRs are available with reverse blocking capability, which adds to the forward voltage drop because of the need to have a long, low doped P1 region. (If one cannot determine which region is P1, a labeled diagram of layers and junctions can help). Usually, the reverse blocking voltage rating and forward blocking voltage rating are the same. The typical application for reverse blocking SCR is in current source inverters.

Noiseless operation owing to absence of moving parts.
Very high switching speed (say $10^9$ operations per second).
High efficiency.
Low maintenance.
Small size and trouble free service for long period.
Large control current range with small gate current of few mA.
Long life as no wear and tear is involved.

14. Explain how UJT acts as a relaxation oscillator

When a voltage (Vs) is firstly applied, the uni junction transistor is “OFF” and the capacitor C1 is fully discharged but begins to charge up exponentially through resistor R3. As the Emitter of the UJT is connected to the capacitor, when the charging voltage Vc across the capacitor becomes greater than the diode volt drop value, the p-n junction behaves as a normal diode and becomes forward biased triggering the UJT into conduction. The uni junction transistor is “ON”. At this point the Emitter to B1 impedance collapses as the Emitter goes into a low impedance saturated state with the flow of Emitter current through R1 taking place.

As the ohmic value of resistor R1 is very low, the capacitor discharges rapidly through the UJT and a fast rising voltage pulse appears across R1. Also, because the capacitor discharges more quickly through the UJT than it does charging up through resistor R3,
the discharging time is a lot less than the charging time as the capacitor discharges through the low resistance UJT.

When the voltage across the capacitor decreases below the holding point of the p-n junction (\( V_{OFF} \)), the UJT turns “OFF” and no current flows into the Emitter junction so once again the capacitor charges up through resistor R3 and this charging and discharging process between \( V_{ON} \) and \( V_{OFF} \) is constantly repeated while there is a supply voltage, \( V_s \) applied.

![Waveform Diagram](image)

The uni junction oscillator continually switches “ON” and “OFF” without any feedback. The frequency of operation of the oscillator is directly affected by the value of the charging resistance R3, in series with the capacitor C1 and the value of \( \eta \). The output pulse shape generated from the Base1 (B1) terminal is that of a saw tooth waveform and to regulate the time period, you only have to change the ohmic value of resistance, R3 since it sets the RC time constant for charging the capacitor.

The time period, \( T \) of the saw toothed waveform will be given as the charging time plus the discharging time of the capacitor. As the discharge time, \( \tau_1 \) is generally very short in comparison to the larger RC charging time, \( \tau_2 \) the time period of oscillation is more or less equivalent to \( T \approx \tau_2 \). The frequency of oscillation is therefore given by \( f = 1/T \).
15. Write a note on phototransistor

A phototransistor is a device that converts light energy into electric energy. Phototransistors are similar to photoresistors but produce both current and voltage, while photoresistors only produce current. This is because a phototransistor is made of a bipolar semiconductor and focuses the energy that is passed through it. Photons (light particles) activate phototransistors and are used in virtually all electronic devices that depend on light in some way.

A phototransistor is a bipolar device that is completely made of silicon or another semi-conductive material and is dependent on light energy. Phototransistors are generally encased in an opaque or clear container in order to enhance light as it travels through it and allow the light to reach the phototransistor’s sensitive parts. A phototransistor has an exposed base that amplifies the light that it comes in contact with. This causes a relatively high current to pass through the phototransistor. As the current spreads from the base to the emitter, the current is concentrated and converted into voltage.
Applications

Phototransistors used in electronic devices senses light. For example, phototransistors are often used in smoke detectors, infrared receivers, and CD players. Phototransistors can also be used in astronomy, night vision, and laser range-finding.

Advantages

They produce a higher current than photodiodes and also produce a voltage, something that photo resistors cannot do. Phototransistors are very fast and their output is practically instantaneous. They are relatively inexpensive, simple, and so small that several of them can fit onto a single integrated computer chip.

Disadvantages:

Phototransistors made of silicon cannot handle voltages over 1,000 Volts. They do not allow electrons to move as freely as other devices, such as electron tubes. Phototransistors are more vulnerable to electrical surges/spikes and electromagnetic energy.

16. Write the characteristics of an ideal operational amplifier

- Infinite input impedance $R_{in}$, and so zero input current.
- Infinite open-loop gain $G = \frac{v_{out}}{v}$. ...
- Zero input offset voltage.
- Infinite voltage range available at the output.
- Infinite bandwidth with zero phase shift and infinite slew rate.
17. Write a note on

(I) Inverting Amplifier

(II) Non inverting Amplifier

Inverting Amplifier:

The operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are:
“No current flows into the input terminal” and that “V1 always equals V2”. However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a “Virtual Earth”. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

1. No Current Flows into the Input Terminals
2. The Differential Input Voltage is Zero as

\[ V1 = V2 = 0 \text{ (Virtual Earth)} \]

\[
\begin{align*}
  i &= \frac{V_{in} - V_{out}}{R_{in} + R_f} \\
  \text{therefore, } i &= \frac{V_{in} - V2}{R_{in}} = \frac{V2 - V_{out}}{R_f} \\
  i &= \frac{V_{in}}{R_{in}} \cdot \frac{V2}{R_{in}} = \frac{V2}{R_{f}} - \frac{V_{out}}{R_{f}} \\
  \text{so, } \frac{V_{in}}{R_{in}} &= \frac{V2}{R_{in} + \frac{1}{R_{f}}} - \frac{V_{out}}{R_f} \\
  \text{and as, } i &= \frac{V_{in} - 0}{R_{in}} = \frac{0 - V_{out}}{R_f} = \frac{0 - V_{out}}{R_{in} \cdot V_{in} - 0} \\
  \text{the Closed Loop Gain (Av) is given as, } \frac{V_{out}}{V_{in}} &= \frac{R_f}{R_{in}}
\end{align*}
\]
Closed-Loop Voltage Gain of an Inverting Amplifier is given as.

\[
\text{Gain (Av)} = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{R_f}{R_{\text{in}}}
\]

Non Inverting Amplifier:

In this circuit the signal is applied to the non-inverting input of the amplifier. However the feedback is taken from the output via a resistor to the inverting input of the operational amplifier where another resistor is taken to ground. It is the value of these two resistors that govern the gain of the operational amplifier circuit.

The gain of the non-inverting amplifier circuit for the operational amplifier is easy to determine. The calculation hinges around the fact that the voltage at both inputs is the same. This arises from the fact that the gain of the amplifier is exceedingly high. If the output of the circuit remains within the supply rails of the amplifier, then the output voltage divided by the gain means that there is virtually no difference between the two inputs.
As the input to the op-amp draws no current this means that the current flowing in the resistors R1 and R2 is the same. The voltage at the inverting input is formed from a potential divider consisting of R1 and R2, and as the voltage at both inputs is the same, the voltage at the inverting input must be the same as that at the non-inverting input. This means that \( \text{Vin} = \text{Vout} \times \frac{R1}{R1 + R2} \). Hence the voltage gain of the circuit \( Av \) can be taken as:

\[
\frac{Vout}{Vin} = Av = 1 + \frac{R2}{R1}
\]

18. Write a note on unity gain buffer

A **unity gain buffer** (also called a unity-gain amplifier) is a op-amp circuit which has a voltage gain of 1. This means that the op amp does not provide any amplification to the signal. The reason it is called a unity gain buffer (or amplifier) is because it provides a gain of 1, meaning there is no gain; the output voltage signal is the same as the input voltage. Thus, for example, if 10V goes into the op amp as input, 10V comes out as output. A unity gain buffer acts as a true buffer, providing no amplification or attenuation to the signal.
A JFET parameters determine its performance in a circuit. The main parameters of a JFET are
(i) a.c. drain resistance
(ii) transconductance
(iii) amplification factor

a.c. drain resistance (rd).

It is the ratio of change in drain source voltage (VDS) to the change in drain current (ID) at constant gate source voltage i.e. a.c. drain resistance,

\[ r_d = \left( \frac{\Delta V_{ds}}{\Delta I_d} \right) V_{GS} \]

Transconductance (gfs).

It is the ratio of change in drain current (ID) to the change in gate source voltage (VGS) at constant drain source voltage i.e. Transconductance,

\[ g_{fs} = \left( \frac{\Delta I_d}{\Delta V_{GS}} \right) V_{DS} \text{ in mA/volt or micromho.} \]

Amplification factor,

\[ \mu = \left( \frac{\Delta V_{ds}}{\Delta V_{gs}} \right) \]

\[ \mu = r_d \times g_{fs} \]

amplification factor = a.c. drain resistance x transconductance
PART-C

1. Draw the circuit diagram of full wave rectifier
   i. With centre tap
   ii. Bridge Connection. Explain their working.

What is the peak inverse voltage of diode in each case.

In the case of centre-tap full wave rectifier, only two diodes are used, and are connected to the opposite ends of a centre-tapped secondary transformer as shown in the figure below. The centre-tap is usually considered as the ground point or the zero voltage reference point.

**Working of Centre-Tap Full Wave Rectifier**

As shown in the figure, an ac input is applied to the primary coils of the transformer.

![Centre-Tap Full-Wave Rectifier Circuit](https://www.CircuitToday.com)

This input makes the secondary ends P1 and P2 become positive and negative alternately. For the positive half of the ac signal, the secondary point D1 is positive, GND point will have zero volt and P2 will be negative. At this instant diode D1 will be forward biased
and diode D2 will be reverse biased. As explained in the Theory Behind P-N Junction and Characteristics of P-N Junction Diode, the diode D1 will conduct and D2 will not conduct during the positive half cycle. Thus the current flow will be in the direction P1-D1-C-A-B-GND. Thus, the positive half cycle appears across the load resistance RLOAD.

During the negative half cycle, the secondary ends P1 becomes negative and P2 becomes positive. At this instant, the diode D1 will be negative and D2 will be positive with the zero reference point being the ground, GND. Thus, the diode D2 will be forward biased and D1 will be reverse biased. The diode D2 will conduct and D1 will not conduct during the negative half cycle. The current flow will be in the direction P2-D2-C-A-B-GND.

---

![output waveform](image)

---

**Peak Inverse Voltage (PIV) of Centre-Tap Full Wave Rectifier:**

PIV is the maximum possible voltage across a diode during its reverse biased period. Let us analyze the PIV of the centre-tapped rectifier from the circuit diagram. During the first half or the positive half of the input ac supply, the diode D1 is positive and thus conducts and provided no resistance at all. Thus, the whole of voltage Vs developed in the upper-half of the ac supply is provided to the load.
resistance RLOAD. Similar is the case of diode D2 for the lower half of the transformer secondary.

Therefore, PIV of D2 = Vm + Vm = 2Vm

PIV of D1 = 2Vm

Centre-Tap Rectifier Circuit Analysis

**Bridge Rectifier Operation**

A single-phase bridge rectifier consists of four diodes and this configuration is connected across the load.

During the Positive half cycle of the input AC waveform diodes D1 and D2 are forward biased and D3 and D4 are reverse biased. When the voltage, more than the threshold level of the diodes D1 and D2, starts conducting – the load current starts flowing through it, as shown as lines path in the diagram below.

![Bridge Rectifier Diagram](image)

During the negative half cycle of the input AC waveform, the diodes D3 and D4 are forward biased, and D1 and D2 are reverse biased. Load current starts flowing through the D3 and D4 diodes when these diodes starts conducting as shown in the figure.
In both the cases, the load current direction is same, i.e., up to down as shown in the figure – so unidirectional, which means DC current. Thus, by the usage of a bridge rectifier, the input AC current is converted into a DC current. The output at the load with this bridge wave rectifier is pulsating in nature, but for producing a pure DC requires additional filter like capacitor.

**Peak Inverse Voltage of a Full wave bridge rectifier:**

Peak inverse voltage (PIV) of a full wave bridge rectifier using the circuit diagram. At any instant when the transformer secondary voltage attains positive peak value Vmax, diodes D1 and D3 will be forward biased (conducting) and the diodes D2 and D4 will be reverse biased (non conducting). For ideal diodes in bridge, the forward biased diodes D1 and D3 will have zero resistance. This means voltage drop across the conducting diodes will be zero. This will result in the entire transformer secondary voltage being developed across load resistance RL.

Thus,

\[
\text{PIV of a bridge rectifier} = V_{\text{max}} \times (\text{max of secondary voltage})
\]

2. **Draw the symbol of Zener Diode. Explain the working of Zener diode with its characteristics and its application as a voltage regulator**

   **Zener Diode** is a single diode connected in a reverse bias. A diode is connected in reverse bias as shown below
Working and Characteristics of Zener Diode

When the diode is connected in forward bias, this diode acts as a normal diode but when the reverse bias voltage is greater than a predetermined voltage zener breakdown voltage takes place. To make the breakdown voltage sharp and distinct, the doping is controlled and the surface imperfections are avoided. In the V-I characteristics above $V_z$ is the zener voltage, It is also the knee voltage because at this point the current is the current is very rapid.
Zener Diode as Voltage Regulator

The term regulator means which regulates or controls. Zener diode can work as a voltage regulator if it is introduced in a circuit. The output across the diode will be constant. It is driven by a current source. As we know if the voltage across the diode exceeds a certain value it would draw excessive current from the supply. The basic diagram of *zener diode as voltage regulator* is given below,

![Diagram of Zener Diode as Voltage Regulator]

To limit the current through the Zener diode series resistance R is introduced whose value can be chosen from the following equation

\[
\text{Resistor value} = \frac{(V_1 - V_2)}{(\text{zener current} + \text{load current})}
\]

The above diagram is of a shunt regulators because the regulating element is parallel to the load. The Zener diode produce a stable reference voltage across the load which fulfills the criteria of regulator.
3. Illustrate the Common Emitter transistor characteristics in detail.

The INPUT CHARACTERISTIC, a graph of base emitter current $I_{BE}$ against base emitter voltage $V_{BE}$ ($I_{BE}/V_{BE}$) shows the input CONDUCTANCE of the transistor. As conductance $1/V$ is the reciprocal of RESISTANCE ($V/I$) this curve can be used to determine the input resistance of the transistor. The steepness of this particular curve when the $V_{BE}$ is above 1 volt shows that the input conductance is very high, and there is a large increase in current for a very small increase in $V_{BE}$. Therefore the input RESISTANCE must be low. Around 0.6 to 0.7 volts the graph curves shows that the input resistance of a transistor varies, according to the amount of base current flowing, and below about 0.5 volts base current ceases.

Input / Output and Mutual Characteristics:

The OUTPUT CHARACTERISTICS gives the value of output conductance. The near horizontal parts of the graph lines show that a change in collector emitter voltage $V_{CE}$ has almost no effect on collector current in this region. Therefore the graph shows that the output resistance of the transistor is high.
The above characteristic graphs shows that, for a silicon transistor with an input applied between base and emitter, and output taken between collector and emitter (a method of connection called common emitter mode. It shows

- Low input resistance (from the input characteristic).
- Fairly high gain (from the transfer characteristic).
- High output resistance (from the output characteristic).

The MUTUAL CHARACTERISTIC shows a graph of MUTUAL CONDUCTANCE $I_C/V_{BE}$ and illustrates the change in collector current with respect to change in base emitter voltage, (i.e. input signal voltage).

<table>
<thead>
<tr>
<th>Content</th>
<th>Definition</th>
<th>Expression (with emitter degeneration)</th>
<th>Expression (without emitter degeneration, i.e., $R_E = 0$)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Current gain</strong></td>
<td>$A_i \triangleq \frac{i_{out}}{i_{in}}$</td>
<td>$\beta$</td>
<td>$\beta$</td>
</tr>
<tr>
<td><strong>Voltage gain</strong></td>
<td>$A_v \triangleq \frac{v_{out}}{v_{in}}$</td>
<td>$r_\pi + \frac{\beta R_C}{\beta + 1 + R_E} \approx -g_m R_C$</td>
<td></td>
</tr>
<tr>
<td><strong>Input impedance</strong></td>
<td>$r_{in} \triangleq \frac{v_{in}}{i_{in}}$</td>
<td>$r_\pi + (\beta + 1) R_E$</td>
<td>$r_\pi$</td>
</tr>
<tr>
<td><strong>Output impedance</strong></td>
<td>$r_{out} \triangleq \frac{v_{out}}{i_{out}}$</td>
<td>$R_C$</td>
<td>$R_C$</td>
</tr>
</tbody>
</table>
4. Derive the expression for h-parameters of transistor

At ac the reactance of coupling capacitors C1 and C2 is so low that they are virtual short circuits, as does the bypass capacitor C3. The power supply (which will have filter capacitors) is also a short circuit as far as ac signals are concerned. The equivalent circuit is shown above on the right hand diagram. The input signal generator is shown as Vs and the generators source impedance as Rs.

As RB1 and RB2 are now in parallel the input impedance will be RB1 $\parallel$ RB2. The collector resistor RC also appears from collector to emitter (as emitter is bypassed).
Parameters are a mix of impedance, admittance and dimensionless units. In common emitter the parameters are:

- $h_{ie}$: input impedance ($\Omega$)
- $h_{re}$: reverse voltage ratio (dimensionless)
- $h_{fe}$: forward current transfer ratio (dimensionless)
- $h_{oe}$: output admittance (Simen)

Lower case suffixes indicate small signal values and the last suffix indicates the mode so $h_{ie}$ is input impedance in common emitter, $h_{fb}$ would be forward current transfer ratio in common base mode, etc. The hybrid model for the BJT in common emitter mode is shown below:

\[
\begin{align*}
\text{v}_{\text{be}} &= h_{ie} i_b + h_{re} \text{v}_{\text{ce}} \\
i_c &= h_{fe} i_b + h_{oe} \text{v}_{\text{ce}}
\end{align*}
\]

The hybrid model is suitable for small signals at mid band and describes the action of the transistor. Two equations can be derived from the diagram, one for input voltage $v_{be}$ and one for the output $i_c$:
If \( i_b \) is held constant (\( i_b = 0 \)) then \( h_{re} \) and \( h_{oe} \) can be solved:
\[
\begin{align*}
  h_{re} &= \frac{v_{be}}{v_{ce}} \mid i_b = 0 \\
  h_{oe} &= \frac{i_c}{v_{ce}} \mid i_b = 0
\end{align*}
\]

Also if \( v_{ce} \) is held constant (\( v_{ce} = 0 \)) then \( h_{ie} \) and \( h_{fe} \) can be solved:
\[
\begin{align*}
  h_{ie} &= \frac{v_{be}}{i_b} \mid v_{ce} = 0 \\
  h_{fe} &= \frac{i_c}{i_b} \mid v_{ce} = 0
\end{align*}
\]

These are the four basic parameters for a BJT in common emitter. Typical values are \( h_{re} = 1 \times 10^{-4} \), \( h_{oe} \) typical value 20uS, \( h_{ie} \) typically 1k to 20k and \( h_{fe} \) can be 50 - 750. The H-parameters can often be found on the transistor datasheets. The table below lists the four h-parameters for the BJT in common base and common collector (emitter follower) mode.

<table>
<thead>
<tr>
<th>Common Base</th>
<th>Common Emitter</th>
<th>Common Collector</th>
<th>Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( h_{rb} )</td>
<td>( h_{ie} )</td>
<td>( h_{rc} )</td>
<td>Input Impedance with Output Short Circuit</td>
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<tr>
<td>( h_{rb} = \frac{v_{be}}{i_b} )</td>
<td>( h_{ie} = \frac{v_{be}}{i_b} )</td>
<td>( h_{rc} = \frac{v_{be}}{i_b} )</td>
<td>Reverse Voltage Ratio Input Open Circuit</td>
</tr>
<tr>
<td>( h_{fb} )</td>
<td>( h_{te} )</td>
<td>( h_{fc} )</td>
<td>Forward Current Gain Output Short Circuit</td>
</tr>
<tr>
<td>( h_{fb} = \frac{i_c}{i_b} )</td>
<td>( h_{te} = \frac{i_c}{i_b} )</td>
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<td>( h_{ob} = \frac{i_c}{v_{ce}} )</td>
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<td>( h_{oc} = \frac{i_c}{v_{ce}} )</td>
<td>Output Admittance Input Open Circuit</td>
</tr>
</tbody>
</table>
5. Write short note on Adder, Subtractor

The adder can be obtained by using either non-inverting mode or differential amplifier. Here the inverting mode is used. So the inputs are applied through resistors to the inverting terminal and non-inverting terminal is grounded. This is called “virtual ground”, i.e. the voltage at that terminal is zero. The gain of this summing amplifier is 1, any scale factor can be used for the inputs by selecting proper external resistors.

1. Connect the circuit as per the diagram.
2. Apply the supply voltages of $+15V$ to pin 7 and pin 4 of IC741 respectively.
3. Apply the inputs $V_1$ and $V_2$ as shown.
4. Apply two different signals (DC/AC) to the inputs.
5. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 adder circuit.
6. Notice that the output is equal to the sum of the two inputs.

**Calculation: Adder**

- $V_o = -(V_1 + V_2)$
- If $V_1 = 2V$ and $V_2 = 2V$, then $V_o = -(2+2) = -4V$. 

**Subtractor:**

The subtracter circuit, input signals can be scaled to the desired values by selecting appropriate values for the resistors. When this is done, the circuit is referred to as scaling amplifier. However in this circuit all external resistors are equal in value. So the gain of amplifier is equal to one. The output voltage $V_o$ is equal to the voltage applied to the non-inverting terminal minus the voltage applied to the inverting terminal; hence the circuit is called a subtractor.

![Subtractor Circuit Diagram]

Connect the circuit as per the diagram.

Apply the supply voltages of $+15V$ to pin7 and pin4 of IC741 respectively. Apply the inputs $V_1$ and $V_2$.

Apply two different signals (DC/AC ) to the inputs. Vary the input voltages and note down the corresponding output at pin 6 of the IC 741 subtractor circuit.

Notice that the output is equal to the difference of the two inputs.

**Calculation: Subtractor**

- $V_o = V_2 - V_1$
- If $V_1=4$ and $V_2 = 2$, then $V_o = 4 - 2 = 2$
Write short note on differentiator and integrator

This Operational Amplifier circuit performs the mathematical operation of Differentiation, ie. “produces a voltage output which is directly proportional to the input voltage’s rate-of-change with respect to time”. In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a “spike” in shape.

A resistor and capacitor forming an RC Network across the operational amplifier and the reactance \( (X_c) \) of the capacitor plays a major role in the performance of a Op-amp Differentiator.

The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, \( X \) resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.
At low frequencies the reactance of the capacitor is “High” resulting in a low gain ( $R_f/X_c$ ) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

At high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate.

$$I_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor = Capacitance x Voltage across the capacitor

$$Q = C \times V_{IN}$$

The rate of change of this charge is

$$\frac{dQ}{dt} = C \frac{dV_{IN}}{dt}$$

but $dQ/dt$ is the capacitor current $i$

$$I_{IN} = C \frac{dV_{IN}}{dt} = I_F$$

$$\therefore \quad -\frac{V_{OUT}}{R_F} = C \frac{dV_{IN}}{dt}$$

$$V_{OUT} = -R_F C \frac{dV_{IN}}{dt}$$

Therefore, the output voltage $V_{out}$ is a constant -$R_f.C$ times the derivative of the input voltage $V_{in}$ with respect to time. The minus sign indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.
A constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependent upon the RC time constant of the Resistor/Capacitor combination.

![Signal Waveforms]

Integrator:

The Op-amp Integrator is an Operational Amplifier circuit that performs the mathematical operation of Integration, the output to respond to changes in the input voltage over time as the op-amp integrator produces an output voltage which is proportional to the integral of the input voltage.

![Op-amp Integrator Diagram]
The magnitude of the output signal is determined by the length of time a voltage is present at its input as the current through the feedback loop charges or discharges the capacitor as the required negative feedback occurs through the capacitor.

When a step voltage, $V_{in}$ is firstly applied to the input of an integrating amplifier, the uncharged capacitor $C$ has very little resistance and acts a bit like a short circuit allowing maximum current to flow via the input resistor, $R_{in}$ as potential difference exists between the two plates. No current flows into the amplifiers input and point X is a virtual earth resulting in zero output. As the impedance of the capacitor at this point is very low, the gain ratio of $X_c/R_{in}$ is also very small giving an overall voltage gain of less than one.

As the feedback capacitor, C begins to charge up due to the influence of the input voltage, its impedance $X_c$ slowly increase in proportion to its rate of charge. The capacitor charges up at a rate determined by the RC time constant, ($\tau$) of the series RC network. Negative feedback forces the op-amp to produce an output voltage that maintains a virtual earth at the op-amp’s inverting input.

Since the capacitor is connected between the op-amp’s inverting input (which is at earth potential) and the op-amp’s output (which is negative), the potential voltage, $V_c$ developed across the capacitor slowly increases causing the charging current to decrease as the impedance of the capacitor increases. This results in the ratio of $X_c/R_{in}$ increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

At this point the capacitor acts as an open circuit, blocking any more flow of DC current. The ratio of feedback capacitor to input
The voltage on the plates of a capacitor is equal to the charge on the capacitor divided by its capacitance giving \( Q/C \). Then the voltage across the capacitor is output \( V_{out} \) therefore: \(-V_{out} = Q/C\). If the capacitor is charging and discharging, the rate of charge of voltage across the capacitor is given as:

\[
V_c = \frac{Q}{C}, \quad V_c = V_x - V_{out} = 0 - V_{out}
\]

\[
\therefore -\frac{dV_{out}}{dt} = \frac{dQ}{Cdt} = \frac{1}{C} \frac{dQ}{dt}
\]

\( dQ/dt \) is electric current and since the node voltage of the integrating op-amp at its inverting input terminal is zero, \( X = 0 \), the input current \( I_{in} \) flowing through the input resistor, \( R_{in} \) is given as:

\[
I_{in} = \frac{V_{in} - 0}{R_{in}} = \frac{V_{in}}{R_{in}}
\]
The current flowing through the feedback capacitor $C$ is

$$I_f = C \frac{dV_{\text{out}}}{dt} = C \frac{dQ}{Cdt} = \frac{dQ}{dt} = \frac{dV_{\text{out}}}{dt}$$

Assuming that the input impedance of the op-amp is infinite (ideal op-amp), no current flows into the op-amp terminal. Therefore, the nodal equation at the inverting input terminal is given as:

$$I_{\text{in}} = I_f = \frac{V_{\text{in}}}{R_{\text{in}}} = \frac{dV_{\text{out}}}{Cdt}$$

$$\therefore \frac{V_{\text{in}}}{V_{\text{out}}} \frac{dt}{R_{\text{in}}C} = 1$$

$$V_{\text{out}} = -\frac{1}{R_{\text{in}}C} \int_0^t V_{\text{in}} dt = -\int_0^t V_{\text{in}} \frac{dt}{R_{\text{in}}C}$$

$$V_{\text{out}} = -\frac{1}{j\omega RC} V_{\text{in}}$$

Where $\omega = 2\pi f$ and the output voltage $V_{\text{out}}$ is a constant $1/RC$ times the integral of the input voltage $V_{\text{in}}$ with respect to time. The minus sign (-) indicates a $180^\circ$ phase shift because the input signal is connected directly to the inverting input terminal of the op-amp.

7. Draw the symbol of MOSFET. Explain the working of MOSFET with its enhancement mode.

[Diagram of MOSFET symbols for N-channel and P-channel]
Construction of an EMOSFET:

The E-MOSFET substrate extends all the way to the silicon dioxide (SiO₂) and no channels are doped between the source and the drain. Channels are electrically induced in these MOSFETs, when a positive gate-source voltage $V_{GS}$ is applied to it.

MOSFET operates only in the *enhancement mode* and has no depletion mode. It operates with large positive gate voltage only. It does not conduct when the gate-source voltage $V_{GS} = 0$. This is the reason that it is called normally-off MOSFET. In these MOSFET’s
drain current $I_D$ flows only when $V_{GS}$ exceeds $V_{GST}$ [gate-to-source threshold voltage].

When drain is applied with positive voltage with respect to source and no potential is applied to the gate two N-regions and one P-substrate from two P-N junctions connected back to back with a resistance of the P-substrate. So a very small drain current that is, reverse leakage current flows. If the P-type substrate is now connected to the source terminal, there is zero voltage across the source substrate junction, and the drain-substrate junction remains reverse biased.

When the gate is made positive with respect to the source and the substrate, negative (i.e. minority) charge carriers within the substrate are attracted to the positive gate and accumulate close to the surface of the substrate. As the gate voltage is increased, more and more electrons accumulate under the gate. Since these electrons can not flow across the insulated layer of silicon dioxide to the gate, so they accumulate at the surface of the substrate just below the gate. These accumulated minority charge carriers N-type channel stretching from drain to source. When this occurs, a channel is induced by forming what is termed an inversion layer (N-type). Now a drain current start flowing. The strength of the drain current depends upon the channel resistance which, in turn, depends upon the number of charge carriers attracted to the positive gate. Thus drain current is controlled by the gate potential.

Since the conductivity of the channel is enhanced by the positive bias on the gate so this device is also called the enhancement MOSFET or E-MOSFET.
The minimum value of gate-to-source voltage $V_{GS}$ that is required to form the inversion layer (N-type) is termed the gate-to-source threshold voltage $V_{GST}$. For $V_{GS}$ below $V_{GST}$, the drain current $I_D = 0$. But for $V_{GS}$ exceeding $V_{GST}$ an N-type inversion layer connects the source to drain and the drain current $I_D$ is large. Depending upon the device being used, $V_{GST}$ may vary from less than 1 V to more than 5 V.

JFETs and DE-MOSFETs are classified as the depletion-mode devices because their conductivity depends on the action of depletion layers. E-MOSFET is classified as an enhancement-mode device because its conductivity depends on the action of the inversion layer. Depletion-mode devices are normally ON when the gate-source voltage $V_{GS} = 0$, whereas the enhancement-mode devices are normally OFF when $V_{GS} = 0$.

Characteristics of an E-MOSFET.

Drain characteristics of an N-channel E-MOSFET are shown in figure. The lowest curve is the $V_{GST}$ curve. When $V_{GS}$ is lesser than $V_{GST}$, $I_D$ is approximately zero. When $V_{GS}$ is greater than $V_{GST}$, the
device turns- on and the drain current $I_D$ is controlled by the gate voltage. The characteristic curves have almost vertical and almost horizontal parts.

The almost vertical components of the curves correspond to the ohmic region, and the horizontal components correspond to the constant current region. Thus E-MOSFET can be operated in either of these regions i.e. it can be used as a variable-voltage resistor (WR) or as a constant current source.

![Transfer Characteristic](image)

**EMOSFET-Transfer Characteristics**

The current $I_{DSS}$ at $V_{GS} \leq 0$ is very small, being of the order of a few nano-amperes. When the $V_{GS}$ is made positive, the drain current $I_D$ increases slowly at first, and then much more rapidly with an increase in $V_{GS}$. The manufacturer sometimes indicates the gate-source threshold voltage $V_{GST}$ at which the drain current $I_D$ attains some defined small value, say 10 u A. A current $I_{D\ (ON)}$ corresponding approximately to the maximum value given on the drain characteristics and the values of $V_{GS}$ required to give this current $V_{GS\ ON}$ are also usually given on the manufacturers data sheet.
8. Write a note on Intrinsic semiconductor and Extrinsic semiconductor

An intrinsic semiconductor material is chemically very pure and possesses poor conductivity. It has equal numbers of negative carriers (electrons) and positive carriers (holes). A silicon crystal is different from an insulator because at any temperature above absolute zero temperature, there is a finite probability that an electron in the lattice will be knocked loose from its position, leaving behind an electron deficiency called a "hole".

If a voltage is applied, then both the electron and the hole can contribute to a small current flow. The conductivity of a semiconductor can be modeled in terms of the band theory of solids. The band model of a semiconductor suggests that at ordinary temperatures there is a finite possibility that electrons can reach the conduction band and contribute to electrical conduction.

The term intrinsic here distinguishes between the
properties of pure "intrinsic" silicon and the dramatically different properties of doped n-type or p-type semiconductors.

**Extrinsic Semiconductor**

Where as an extrinsic semiconductor is an improved intrinsic semiconductor with a small amount of impurities added by a process, known as doping, which alters the electrical properties of the semiconductor and improves its conductivity. Introducing impurities into the semiconductor materials (doping process) can control their conductivity.

Doping process produces two groups of semiconductors: the negative charge conductor (n-type) and the positive charge conductor (p-type). Semiconductors are available as either elements or compounds. Silicon and Germanium are the most common elemental semiconductors. Compound Semiconductors include InSb, InAs, GaP, GaSb, GaAs, SiC, GaN. Si and Ge both have a crystalline structure called the diamond lattice. That is, each atom has its four nearest neighbors at the corners of a regular tetrahedron with the atom itself being at the center. In addition to the pure element semiconductors, many alloys and compounds are semiconductors. The advantage of compound semiconductor is that they provide the device engineer with a wide range of energy gaps and mobilities, so that materials are available with properties that meet specific requirements. Some of these semiconductors are therefore called wide band gap semiconductors.
The addition of pentavalent impurities such as antimony, arsenic or phosphorous contributes free electrons, greatly increasing the conductivity of the intrinsic semiconductor. Phosphorous may be added by diffusion of phosphine gas (PH3).

P-Type Semiconductor
The addition of trivalent impurities such as boron, aluminum or gallium to an intrinsic semiconductor creates deficiencies of valence electrons, called "holes". It is typical to use B\(_2\)H\(_6\) diboron gas to diffuse boron into the silicon material.